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Simplifying Post-Silicon Diagnostics Using Large Language Models for Advanced Node Yield Improvement

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Abstract

The semiconductor industry faces significant challenges in post-silicon diagnostics as manufacturing processes advance toward smaller technology nodes, where increased integration complexity leads to exponentially growing defect types and reliability concerns that substantially impact product yield. Traditional diagnostic approaches require extensive collaboration across multiple engineering disciplines and often consume several days or weeks to isolate root causes of failures, creating bottlenecks in production ramp-up and delaying corrective actions. This article investigates the integration of Large Language Models into silicon diagnostics workflows, where LLMs function as intelligent database readers and analysis tools capable of processing vast amounts of technical data from diverse sources, including design rule checks, timing analysis reports, power integrity assessments, and automated test equipment failure logs. The proposed methodology encompasses comprehensive training of LLM systems using critical design verification data across multiple domains, enabling the models to understand intricate relationships between design choices, manufacturing constraints, and potential failure mechanisms. The diagnostic workflow leverages the LLM's capacity to correlate failure information with design characteristics, highlighting relevant timing paths, voltage drop hotspots, and cell behaviors associated with failing regions in minutes rather than the days typically required for manual analysis. Beyond diagnostics, the LLM suggests targeted scan pattern generation strategies based on identified defect characteristics and provides root cause analysis capabilities that distinguish between systematic and random defect patterns. The continuous learning framework ensures that diagnostic capabilities evolve alongside manufacturing technology advancements, with each silicon revision and technology node contributing additional training data that enhances the model's predictive accuracy and expands its understanding of failure mechanisms, ultimately transforming the LLM into a dynamic knowledge management system that accelerates time-to-market and improves profitability for advanced semiconductor products.

Keywords: Large Language Models, Post-Silicon Diagnostics, Semiconductor Yield Improvement, Scan-Based Testing, Continuous Learning Framework

Introduction

The semiconductor industry faces mounting challenges as manufacturing processes advance toward smaller technology nodes. With increased integration complexity comes a corresponding rise in defect types and reliability concerns that can significantly impact product yield. As technology nodes shrink below the nanometer scale, the number of potential defect mechanisms increases exponentially, with studies indicating that defect density can vary by orders of magnitude depending on process maturity and manufacturing controls. Traditional diagnostic approaches for identifying silicon process variations require extensive collaboration across multiple engineering disciplines, often consuming several days or weeks to isolate root causes of failures. This time-intensive process creates bottlenecks in production ramp-up and delays corrective actions needed to improve manufacturing yields.

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Scan-based testing has become the cornerstone of modern semiconductor diagnostics, with scan chains inserted into sequential elements to improve observability and controllability. The diagnostic effectiveness of scan architectures depends critically on the ability to isolate fault locations with precision, particularly when dealing with complex failure scenarios involving multiple defect sites within scan chain structures. Research addressing scan chain diagnosis has explored methodologies for efficiently identifying stuck-at faults, which represent one of the most common defect types encountered in manufacturing [1]. These stuck-at faults occur when circuit nodes become permanently fixed at logic high or logic low values due to manufacturing imperfections, process variations, or contamination during fabrication. The diagnostic resolution—defined as the ability to pinpoint the exact location and type of defect—depends critically on the quality of scan pattern generation, the comprehensiveness of failure data collected from automated test equipment, and the sophistication of diagnostic algorithms employed. However, even with optimized scan architectures, the process of correlating tester failure patterns with physical design characteristics, timing violations, and process-induced defects remains labor-intensive and requires deep expertise across multiple domains, including design-for-test, physical implementation, and foundry process technology.

The emergence of Large Language Models represents a paradigm shift in how engineering teams can approach post-silicon diagnostics. These advanced artificial intelligence systems possess sophisticated natural language understanding and inference capabilities that enable them to process vast amounts of technical data from various sources. The application of machine learning techniques and artificial intelligence in diagnostic contexts has expanded beyond traditional semiconductor applications, with recent developments demonstrating the power of integrating diverse data sources for enhanced decision-making in complex technical domains [2]. By leveraging LLMs as intelligent database readers and analysis tools, diagnostic workflows can be streamlined significantly. This methodology transforms how engineers interact with critical design data, timing analysis reports, and tester failure logs, providing rapid insights that previously required manual correlation across multiple tool outputs and team expertise. The LLM's ability to synthesize information from disparate sources—including static timing analysis reports showing setup and hold violations, electromigration and IR drop analysis highlighting power integrity concerns, and scan diagnostic outputs identifying probable fault locations—creates a unified analytical framework that accelerates root cause identification and enables faster implementation of yield improvement strategies.

Methodology for LLM-Based Silicon Diagnostics

Training Phase and Data Preparation

The foundation of this diagnostic approach begins with comprehensive training of LLM systems using critical design rule checks from multiple verification domains. The models ingest information from design-for-test constraints, clock tree synthesis reports, static timing analysis outputs, electromigration and IR drop assessments, and physical implementation data specific to target technologies. This training phase establishes the baseline knowledge that enables the LLM to understand the intricate relationships between design choices, manufacturing constraints, and potential failure mechanisms. The complexity of modern integrated circuits necessitates that the LLM be exposed to extensive datasets encompassing various aspects of the design flow, from initial architectural decisions through final physical implementation and verification signoff. As semiconductor technology has evolved from planar transistor architectures to three-dimensional structures, the physical design considerations have become

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increasingly complex, requiring a sophisticated understanding of device physics, parasitic effects, and process-induced variations that significantly impact circuit performance and yield [3].

A crucial aspect of this training involves exposing the models to threshold values for critical rules across different technology nodes. The LLM learns to recognize patterns in how various cell types—such as low-threshold voltage cells with faster switching characteristics versus high-threshold voltage cells optimized for power efficiency—behave under different operating conditions. The transition from traditional planar transistors to advanced three-dimensional device structures has introduced new challenges in physical design and implementation, with critical dimensions shrinking to unprecedented scales and requiring careful attention to electrostatic control, short-channel effects, and variability management [3]. The training datasets include parametric information about cell delays, transition times, and power consumption profiles across multiple process corners, enabling the LLM to correlate physical design choices with potential reliability risks. Dynamic voltage drop analysis reports further enrich the model's understanding of peak current demands and power integrity requirements that influence circuit reliability. These reports capture transient voltage fluctuations that occur during circuit switching, identifying regions where supply voltage may drop below acceptable thresholds and potentially cause timing failures or functional errors.

The training methodology incorporates structured data from automated test pattern generation tools, which provide insights into fault coverage metrics and the relationship between test patterns and defect detection capabilities. Recent developments in machine learning applications for hardware security and design verification have demonstrated the effectiveness of integrating artificial intelligence techniques with traditional electronic design automation workflows [4]. By training on historical correlation data between scan diagnostic results and actual silicon failure analysis findings, the LLM develops an understanding of common defect signatures and their manifestations in test data. This includes learning to recognize patterns associated with bridging defects where adjacent metal lines create unintended connections, open defects where interconnects are incompletely formed, and parametric defects where circuit elements function but fail to meet timing or power specifications. The model also ingests information about design-dependent effects such as crosstalk-induced noise, process-dependent threshold voltage variations, and temperature-dependent performance degradation, building a comprehensive knowledge base that enables intelligent correlation of multiple failure indicators during the diagnostic phase.

Verification Domain	Data Type	Key Parameters	Failure Mechanisms Addressed	Impact on Diagnostic Accuracy
Design-for-Test	Scan chain structure, fault coverage metrics	Test pattern count, coverage percentage	Stuck-at faults, transition faults	High - enables fault localization
Clock Tree Synthesis	Clock distribution network, skew reports	Clock skew values, insertion delay	Timing violations, hold time failures	Medium - identifies timing-related defects
Static Timing Analysis	Critical path reports, setup/hold margins	Slack values, path delays	At-speed defects, parametric failures	High - correlates timing with failures
Electromigration	Power grid	Peak current	Power integrity	High - identifies

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& IR Drop	analysis, voltage drop maps	demand, voltage drop magnitude	issues, functional errors	power-related vulnerabilities
Physical Implementation	Cell placement, routing density	Layer assignments, spacing violations	Bridging defects, open defects	High - links physical design to defects
Cell Library Characterization	LVT/HVT cell behavior, delay profiles	Transition times, power consumption	Process variation sensitivity	Medium - understands cell-level behavior
Historical Failure Data	Silicon failure analysis results	Defect types, failure signatures	All defect categories	Very High - learns from past diagnostics

Table 1: LLM Training Data Sources and Their Diagnostic Contributions [3, 4]

Diagnostic Workflow Integration

Once trained, the LLM receives design rule check logfiles and comprehensive timing path reports as inputs. The system processes information about critical timing paths, analyzing setup and hold time margins across different process corners and operating modes. By understanding the cell libraries utilized in specific designs, including mixed threshold voltage implementations, the LLM builds a contextual map of potential vulnerability points within the circuit architecture. The analysis encompasses multiple operating scenarios, including typical, best-case, and worst-case process corners, as well as variations in supply voltage and temperature that can significantly affect timing closure and circuit reliability. The LLM's ability to parse and interpret complex timing reports enables it to identify critical paths that are most susceptible to process variations, manufacturing defects, or operational stress conditions.

When scan diagnostic methods identify fault sites based on automated test equipment failure logs, these locations are provided to the LLM along with their hierarchical instance paths. The model then correlates this failure information with the design characteristics it has learned, highlighting relevant timing paths, voltage drop hotspots, and cell behaviors associated with the failing regions. Advanced scan chain diagnostic methodologies have been developed to efficiently isolate fault locations within scan structures, employing symbolic simulation techniques that can process failure signatures and identify defective scan cells with high accuracy while minimizing computational overhead [5]. The scan chain diagnostic process generates detailed failure signatures that indicate which flip-flops or logic elements within the scan path are exhibiting faulty behavior, whether due to stuck-at faults, transition delay faults, or other defect mechanisms. This correlation happens in minutes rather than the days typically required for manual analysis across distributed engineering teams. The LLM leverages its trained understanding of design implementation details to quickly identify relationships between the failing scan cells and their surrounding logic, associated power distribution networks, and clock tree structures that might contribute to the observed failures.

The integration workflow benefits from the LLM's capacity to process multiple data streams simultaneously, including static timing analysis reports that capture setup and hold violations, power grid analysis outputs that reveal IR drop concerns, and physical design databases that contain placement and routing information. As semiconductor technology scales into the nanoscale regime, reliability challenges have become increasingly critical, with factors such as process variations, aging effects, soft errors from radiation, and interconnect reliability issues significantly impacting circuit dependability and requiring comprehensive reliability-aware design methodologies and diagnostic approaches [6]. The LLM synthesizes these diverse inputs to generate comprehensive diagnostic reports that guide engineering

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teams toward probable root causes, whether they stem from design weaknesses, manufacturing process issues, or interactions between multiple factors. By automating the correlation of failure data with design characteristics, the LLM-based diagnostic workflow eliminates much of the manual effort traditionally required to navigate through multiple tool outputs, cross-reference hierarchical design databases, and coordinate analysis across functional verification, physical design, and test engineering disciplines. This streamlined approach accelerates the feedback loop between silicon test results and corrective design or process modifications, directly contributing to faster yield ramp and reduced time-to-market for advanced semiconductor products.

Input Data Stream	Information Content	Analysis Performed	Output Generated	Processing Time	Traditional Method Time
Design Rule Check Logfiles	Violation reports, spacing issues	Rule compliance verification	Vulnerability hotspot map	Minutes	Hours to days
Timing Path Reports	Set up/hold margins, slack values	Multi-corner timing analysis	Critical path identification	Minutes	Hours to days
Cell Library Data	LVT/HVT characteristics, delays	Threshold voltage impact assessment	Cell behavior correlation	Minutes	Hours
ATE Failure Logs	Scan pattern failures, bit positions	Fault signature analysis	Defect location isolation	Minutes	Days to weeks
Hierarchical Instance Paths	Design topology, logic relationships	Structural correlation	Failure propagation analysis	Minutes	Days
Power Grid Analysis	IR drop values, current density	Power integrity assessment	Voltage drop hotspot identification	Minutes	Hours to days
Physical Design Database	Placement, routing, layer info	Spatial defect correlation	Physical vulnerability mapping	Minutes	Days
Process Corner Data	Typical/best/worst case parameters	Multi-scenario timing validation	Margin sensitivity analysis	Minutes	Hours to days

Table 2: LLM Diagnostic Workflow Data Processing Capabilities [5, 6]

Pattern Generation and Root Cause Analysis

Beyond diagnostics, the LLM suggests targeted scan pattern generation strategies based on identified defect characteristics. For bridging defects where adjacent nets may be inadvertently connected, the model recommends specific test patterns that maximize detection probability. Similarly, for at-speed defects occurring at functional clock frequencies, the LLM proposes timing-sensitive patterns that stress the relevant paths. This intelligent pattern generation focuses testing efforts on the most probable failure

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mechanisms, reducing debug time and improving defect coverage. The LLM analyzes the spatial relationships between signal lines in the physical layout, considering factors such as metal layer assignments, routing density, and minimum spacing violations that might predispose certain nets to bridging failures. By understanding the electrical characteristics of potential bridging scenarios—whether resistive bridges with varying impedance values or hard shorts that create direct connections—the model can propose test patterns that apply complementary logic values to adjacent nets, maximizing the observability of bridging-induced failures at scan outputs.

The methodology proves particularly effective for various defect categories, including stuck-at faults, transition faults, and memory-related failures. The evolution of semiconductor packaging technologies has introduced new complexities in fault isolation and failure analysis, requiring advanced techniques that can address the challenges posed by high-density interconnects, three-dimensional integration, and the increasing use of advanced packaging approaches that integrate multiple dies within a single package [7]. Stuck-at faults, which manifest as circuit nodes permanently fixed at logic zero or logic one regardless of intended switching activity, require test patterns that attempt to set the faulty node to the opposite logic value and propagate the resulting error to observable points. Transition faults, which prevent proper logic transitions due to timing-related defects or resistive opens, necessitate at-speed testing where patterns are applied at functional clock frequencies to expose delays that might not be detected during slower scan-shift operations. By maintaining a comprehensive understanding of both the design implementation and the failure symptoms, the LLM bridges the knowledge gap that typically exists between test engineers, design teams, and foundry process experts.

The root cause analysis capability of the LLM extends to understanding systematic versus random defect patterns, enabling identification of whether failures stem from design marginalities that affect multiple dies consistently or from random manufacturing variations that produce unique failure signatures across different units. Research in microelectronics reliability has established comprehensive frameworks for understanding failure mechanisms in integrated circuits, with particular emphasis on the physical and chemical processes that lead to device degradation, the statistical methods for analyzing failure data, and the testing methodologies required to ensure long-term reliability under various stress conditions, including temperature cycling, humidity exposure, and electrical overstress [8]. The LLM correlates observed failure patterns with known defect mechanisms, drawing upon its training data that encompasses physical failure analysis findings, electrical characterization results, and historical yield learning from previous product generations. This comprehensive perspective enables the model to distinguish between defects originating from mask design issues, lithography limitations, chemical-mechanical polishing non-uniformities, or contamination events during fabrication. By providing this level of insight, the LLM-based approach facilitates more targeted corrective actions, whether through design modifications to improve robustness margins, process recipe adjustments to optimize manufacturing windows, or enhanced test pattern development to improve defect screening efficiency.

Defect Type	Physical Characteristic	Pattern Generation Strategy	Test Approach	Detection Optimization	Debug Time Reduction
Bridging Defects	Adjacent nets inadvertently connected	Complementary logic value application	Spatial layout analysis	Maximize observability at scan outputs	High - targeted pattern focus

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Resistive Bridges	Varying impedance connections	Multiple drive strength patterns	Electrical characteristic modeling	Apply different voltage levels	Medium to High
Hard Shorts	Direct metal-to-metal connections	Strong opposite-value patterns	Metal layer assignment analysis	Direct signal conflict creation	Very High
At-Speed Defects	Functional clock frequency failures	Timing-sensitive stress patterns	Critical path targeting	Functional frequency application	High - path-specific testing
Stuck-at Faults	Nodes fixed at logic 0 or 1	Opposite value setting and propagation	Controllability and observability	Error propagation to scan cells	High - comprehensive coverage
Transition Faults	Prevented logic transitions	At-speed functional testing	Timing defect isolation	Functional clock frequency patterns	High - delay detection
Memory-Related Failures	Storage element defects	Pattern-sensitive test sequences	BIST and diagnostic patterns	Address and data pattern variations	Medium to High

Table 3: LLM-Guided Test Pattern Generation Strategies for Defect Categories [7, 8]

Continuous Learning and Model Refinement

One of the most crucial benefits of such an approach is in its ability to be improved continuously. The models of the LLM are sustained by experience and are modified with new process problems that are identified and solved to form an ever-expanding database of diagnostic know-how. The predictive accuracy of the model and the knowledge of failure mechanisms are improved with each silicon revision and each new technology node. Such a process of iterative refinement is what makes diagnostic capability keep up with the development of manufacturing technology. The silicon test result feedback system with failure analysis results and model updates provides a self-perfecting mechanism that the results of the diagnostic cycle improve the outcomes of the next diagnostic cycle. Such validated information is added to the knowledge base of the LLM as the engineering teams discover root causes and apply corrective measures, whereupon the pattern is noticed more quickly by the model in subsequent diagnostic cases, and also whereupon more specific investigation strategies are proposed in subsequent diagnostic cases, depending on the learning that has been received by cases previously.

The continuous learning model resolves one of the bedrock issues of semiconductor diagnostics that is the rapid change of both technologies of manufacturing and mechanisms of fault as the process nodes are improved. The recent progress in the use of large language models in hardware design and verification has shown that these systems can comprehend technical documentation of complex systems, interpret design requirements, and make intelligent suggestions on how to improve design quality and test coverage [9]. The learning nature of the model means that when rare or new forms of defects are experienced, and the characteristics are stored in its long-term memory, the system acquires the new information permanently, and in future products or technological generations, the time it takes to diagnose a similar problem is reduced. This experience is especially useful in the event of switching to new process nodes, where most underlying design and production concepts can still be used in spite of the fact that certain parameters and constraints actually change. The LLM is capable of using the experience of the

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failure mechanisms of mature technologies to minimize the learning curve of emerging nodes by determining the areas of vulnerability in the new generation, based on similar circumstances in the older generation.

Another advantage of the refinement process is the cross-functional knowledge that is integrated during the process, since the LLM takes into consideration the knowledge of various fields of engineering. The future of machine learning has indicated potential in streamlining complex engineering tasks (manufacturing and quality control are examples where machine learning algorithms can reveal patterns in massive datasets and deliver actionable recommendations on improving the process) [10]. The LLM can build a more sophisticated level of understanding of the complex relationship among these realms by continually updating its training data with the information obtained in the course of the design revisions that resolved the observed weaknesses, process improvements to eliminate systematic defect sources, and improved test patterns to increase the fault coverage. It is this broad view that allows the model to offer more detailed recommendations that not only take into account the immediate diagnosis results but also what the results imply in terms of design robustness, manufacturing yield optimization, and test cost reduction. The sustained learning capacity is what makes the LLM more of a dynamic knowledge management system that not only captures and spreads organizational learning across product lines, technology nodes, and engineering teams, but also helps increase the speed of time-to-market and profitability of advanced semiconductor products.

Learning Phase	Data Source	Knowledge Type	Model Enhancement	Diagnostic Improvement	Time-to-Diagnosis Reduction
Initial Silicon Revision	First test results, failure logs	Baseline defect patterns	Initial failure mechanism mapping	Establishes foundation	Baseline
Root Cause Identification	Failure analysis findings	Validated defect correlations	Confirmed pattern recognition	Increased accuracy	20-30% faster
Corrective Action Implementation	Design/process modifications	Solution effectiveness data	Preventive strategy learning	Proactive vulnerability detection	30-40% faster
Subsequent Silicon Revisions	Updated test data, new failures	Evolved defect signatures	Expanded failure mechanism library	Rare defect recognition	40-50% faster
Technology Node Transition	New node characteristics	Cross-generation principles	Analogous situation identification	Accelerated learning curve	50-60% faster
Cross-Functional Integration	Multi-discipline insights	Holistic system understanding	Complex relationship modeling	Nuanced recommendations	60-70% faster

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Mature Knowledge Base	Comprehensive historical data	Organizational learning repository	Predictive capability enhancement	Proactive issue prevention	70-80% faster

Table 4: Continuous Learning Framework - Knowledge Accumulation and Model Evolution [9, 10]

Conclusion

The implementation of Large Language Models in post-silicon diagnostics is an innovative breakthrough in the semiconductor yield enhancement procedures that are associated with advanced technology nodes. This article shows that diagnostics using the LLM can play a very important role in simplifying the traditionally intensive process of detecting variations in silicon processes by playing an intelligent mediatory role between the complex design databases and engineering analysis. The LLM, through extensive training on important design rule checks, timing analysis results, power integrity checks, and other contextual failure information, acquires complex insights into the complex interplay between design implementation decisions, production limitations, and defect mechanisms. The diagnostic workflow integration allows the automatic test equipment failures to be quickly correlated with the design characteristics, and the timing to analyze a defect is shortened to only minutes, with the diagnostic accuracy of the different defect types, such as stuck-at faults, bridging defects, transition faults, and memory-related failures, remaining high. The ability of the methodology to generate scan patterns under the conditions of the known defect characteristics is an added benefit in terms of efficiency in testing, since it enables concentrating efforts on the most likely failure modes. The lifelong learning model makes sure that the system grows as the manufacturing technology develops and every diagnostic interaction adds the verified knowledge to the growing base of expertise that is especially useful in times of the changes of the technology node. The integration of cross-functional lessons of design, test, physical implementation, process engineering, and failure analysis disciplines into the LLM makes it more of a dynamic knowledge management system than a static analysis tool that helps capture and transfer organizational learning across product lines and engineering teams. This holistic method not only shortens the feedback loop between silicon test results and corrective actions, but also allows more subtle recommendations that take into consideration larger implications of design robustness and manufacturing yield optimization, and test cost reduction, and essentially leads to faster yield ramp, shorter time-to-market, and increased profitability of cutting-edge semiconductor products in a more competitive industry environment.

References

[1] Sunghoon Kim et al., "Scan Chain Architecture With Data Duplication for Multiple Scan Cell Fault Diagnosis," IEEE Xplore, 2022, https://ieeexplore.ieee.org/document/9964073

[2] Juan F Gaitan Guerrero et al., "A novel fine-tuning and evaluation methodology for large language models on IoT raw data summaries (LLM-RawDMeth): A joint perspective in diabetes care," ScienceDirect, September 2025. https://www.sciencedirect.com/science/article/pii/S0169260725002950

[3] Ramalinga Reddy Kotapati et al., "Physical Design Evolution and Implementation Strategies for Advanced FinFET and Gate-All-Around Technologies: A Comprehensive Review," ResearchGate, December 2024. https://www.researchgate.net/publication/387583328_PHYSICAL_DESIGN_EVOLUTION_AND_IMPLEMENTATION_STRATEGIES_FOR_ADVANCED_FINFET_AND_GATE-ALL-AROUND_TECHNOLOGIES_A_COMPREHENSIVE_REVIEW

10.48047/jocaaa.2026.35.03.16

[4] Manisha Kumari et al., "Machine Learning Applications in Hardware Security and Design Verification," IEEE Xplore, 2025. https://ieeexplore.ieee.org/document/11141575

[5] Sunghoon Chun et al., "An Efficient Scan Chain Diagnosis Method Using a New Symbolic Simulation," ResearchGate, April 2008. https://www.researchgate.net/publication/4335578_An_Efficient_Scan_Chain_Diagnosis_Method_Using_a_New_Symbolic_Simulation

[6] Alexandre Schmid et al., "Reliability of nanoscale circuits and systems: Methodologies and circuit architectures," ResearchGate, January 2011. https://www.researchgate.net/publication/287554400_Reliability_of_nanoscale_circuits_and_systems_Methodologies_and_circuit_architectures

[7] Mario Pocheko et al., "Advanced Fault Isolation and Failure Analysis Techniques for Future Package Technologies," ResearchGate, November 2005. https://www.researchgate.net/publication/237461686_Advanced_Fault_Isolation_and_Failure_Analysis_Techniques_for_Future_Package_Technologies

[8] Jiann Min Chin et al., "Fault isolation in semiconductor product, process, physical and package failure analysis: Importance and overview," ScienceDirect, November 2011. https://www.sciencedirect.com/science/article/abs/pii/S0026271411002605

[9] Avinash Patil, "Large Language Models for Hardware Design and Verification," arXiv, 2025, https://arxiv.org/pdf/2505.13766

[10] Heliyon., "Machine Learning Applications in Manufacturing Process Optimization," Sciencedirect, 2024, https://www.sciencedirect.com/science/article/pii/S2405844024159324